



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,149	07/24/2003	Gerald R. Stanley	11336/513 (P03087US)	9305

27879	7590	10/19/2007
INDIANAPOLIS OFFICE 27879		
BRINKS HOFER GILSON & LIONE		
ONE INDIANA SQUARE, SUITE 1600		
INDIANAPOLIS, IN 46204-2033		

EXAMINER	
HAN, YOUNGHUJE JESSICA	

ART UNIT	PAPER NUMBER
2838	

NOTIFICATION DATE	DELIVERY MODE
10/19/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentofficeactions@brinkshofer.com
svessely@usebrinks.com
dhasler@usebrinks.com

Office Action Summary

Application No.

10/626,149

Applicant(s)

STANLEY, GERALD R.

Examiner

Y. J. Han

Art Unit

2838

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 September 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-39 and 47-62 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-39 and 47-62 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☐ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 8/17/07.
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date: _____.
- ☐ Notice of Informal Patent Application
- ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-6, 34-39, 47-50, and 52-62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barbosa et al (disclosed in IDS filed on 03/28/06) in view of Huang et al (disclosed in IDS filed on 03/28/06) and Cyr (5,870,294).

Barbosa et al discloses the invention substantially as claimed including a power factor correcting power supply comprising: a first boost converter (S1); a second boost converter (S2) coupled in series with the first boost converter, where the first and second boost converters are configured to receive an input voltage and supply a boost voltage (see Fig. 3). Barbosa et al, however, does not disclose two coupled boost sub-circuits for each of the converters and a power factor controller configured to control boost converters with pulse modulation. First, Huang et al teaches that the use of coupled boost sub-circuits is well known in the art. See Fig. 1a. Second, Fig. 1 of Cyr shows Power Factor Controller 22 with a boost topology driven by conditional PWM drive signals output by a gate array logic IC 24. Thus, it would have been obvious to one having ordinary skill in the art to employ two coupled boost sub-circuits of Huang et al and the power factor correction controller of Cyr in Barbosa et al to obtain the claimed invention for the purpose of minimizing the component stresses.

Art Unit: 2838

3. Claims 7-11 and 13-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barbosa et al in view of Huang et al and Cyr (5,870,294), and further in view of Guerrero (5,923,152).

Barbosa et al as modified by Huang et al and Cyr discloses the invention substantially as claimed but does not disclose boost switches which are independently switchable. Guerrero teaches clearly that the use of independently controlled switches (40, 46, 80, and 88 in Fig. 5) for obtaining the desired output voltage in the power factor correction circuit is well known in the art. Thus, it would have been obvious to one having ordinary skill in the art to employ independently controlled switches in Barbosa et al as modified by Huang et al and Cyr, as taught by Guerrero, to obtain the claimed invention for the purpose of achieving highly efficient converter that minimizes harmonics and EMI problems.

4. Claims 12, 19-33, and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barbosa et al in view of Huang et al and Cyr, and further in view of Pinheiro et al (disclosed in IDS filed on 03/28/06).

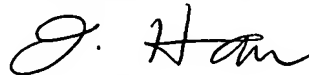
Barbosa et al as modified by Huang et al and Cyr discloses the invention substantially as claimed but does not disclose converter configured to balance the boost voltage. Pinheiro et al teaches that the use of boost power factor correction configured to balance the boost voltage is well known in the art. Thus, it would have been obvious to one having ordinary skill in the art to employ the balancing of the boost voltage in Barbosa et al as modified by Huang et al and Cyr, as taught by Pinheiro et al, to obtain the claimed invention for the purpose of achieving highly efficient converter that minimizes input current ripple.

Art Unit: 2838

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Y. J. Han whose telephone number is 571-272-2078. The examiner can normally be reached on Mon-Fri 6:30am-3:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hezron Williams can be reached on 571-272-2208. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



J. Han
Primary Examiner
Art Unit 2838